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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,660	04/12/2001	Luan C. Tran	MI22-1637	6625

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EXAMINER
SCHILLINGER, LAURA M

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

		Application No.	Applicant(s)
	Office Action Summary	09/834,660	TRAN, LUAN C.
		Examiner	Art Unit	
		Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _02 May 2006_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _21-30 and 61-104_ is/are pending in the application.

    4a) Of the above claim(s) _83-104_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _21-30 and 61-82_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _5/2/06_, '/15/03

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

Applicant's oath swears behind the Liaw reference; however other art has been

discovered which anticipates Applicant's claim language.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
patent by another filed in the United States before the invention by the applicant for patent, except that an
international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
subsection of an application filed in the United States only if the international application designated the United
States and was published under Article 21(2) of such treaty in the English language.

Claims 21-30, 61-82 are rejected under 35 U.S.C. 102(b) as being anticipated by Liou et

al ('268).

In reference to claim 21, Liou et al teaches a method comprising:

Forming two series of FETs over a substrate (Fig.1f), one being isolated from adjacent

devices by STI, the other having active area widths greater than 1um and , the one series being

formed to have active area widths less than 1 um (Col.7, lines: 60-65) to achieve lower threshold

voltages (TVs) than the other of the series (inherent-see Schuegraf et al ('976)- teaching that the

trench isolation effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 22, Liou et al teaches wherein the TVs for the 2 series of FETS are defined by a common channel implant (Col.5, lines: 1-10) inherent-see Schuegraf et al ('976)- teaching that the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 23, Liou et al teaches wherein the threshold voltages for the two series of FETs are defined by a common channel implant, the implant being the only channel implant which defines the TVs for the two series of FETs (Col.5, lines: 1-10 inherent-see Schuegraf et al ('976)- teaching that the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 24, Liou et al teaches wherein the TVs for the two series of FETs are defined by one or more common channel implants (Col.5, lines: 1-10 inherent-see Schuegraf et al ('976)- teaching that the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 25, Liou et al teaches wherein the TVs for the two series of FETs are defined by one or more common channel implants, the common channel implants being the only channel implants which define the TV for the two series of FETs (Col.5, lines: 1-10 inherent-see Schuegraf et al ('976)- teaching that the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 26, Liou et al teaches a method of forming two series of FETs over a substrate (Fig.2F one being isolated from adjacent devices by STI (Fig.2f (28)) and achieving different TVs by varying the active widths of the FETs in the series providing a first series of

transistors having active area widths less than active area widths of a second series of transistors

and wherein the threshold voltages of the transistors of the first series are less than the threshold

voltages of the transistors of the second series, at least one series having active area widths less

than one micron (Col.7, lines: 60-65- inherent- see Schuegraf et al ('976)- teaching that the

trench isolation effects the threshold voltage (Col.2, lines: 35-45).

In reference to claim 27, Liou et al teaches wherein the TVs for the 2 series of FETS are defined

by a common channel implant (Col.5, lines: 1-10 inherent-see Schuegraf et al ('976)- teaching

that the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 28, Liou et al teaches wherein the threshold voltages for the two series of

FETs are defined by a common channel implant, the implant being the only channel implant

which defines the TVs for the two series of FETs (Col.5, lines: 1-10 inherent-see Schuegraf et al

('976)- teaching that the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 29, Liou et al teaches wherein the TVs for the two series of FETs are

defined by one or more common channel implants (Col.5, lines: 1-10 inherent-see Schuegraf et

al ('976)- teaching that the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 30, Liou et al teaches wherein the TVs for the two series of FETs are

defined by one or more common channel implants, the common channel implants being the only

channel implants which define the TV for the two series of FETs (Col.5, lines: 1-10).

In reference to claim 61, Liou et al teaches wherein the transistors of the two series comprise

transistors having a single geometry type (Fig.2f)

In reference to claim 62, Liou et al teaches wherein the transistors of the single geometry type

comprise planar transistors (Fig.2f).

In reference to claim 63, further comprising performing a common channel implant within active

areas of the transistors of the two series at the same moment in time (Col.5, lines: 1-10).

64. The semiconductor processing method of claim 21, further comprising performing a common

channel implant within active areas of both of the series of the transistors at the same moment in

time to define the different threshold voltages of the transistors of the two series (Col.5, lines: 1-

10 inherent-see Schuegraf et al ('976)- teaching that the substrate doping effects the threshold

voltage (Col.2, lines: 35-45)).).

65. The semiconductor processing method of claim 64, wherein the common channel implant is

the only channel implant which defines the different threshold voltages of the transistors of the

two series (Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that the substrate

doping effects the threshold voltage (Col.2, lines: 35-45)).

66. Liou teaches the semiconductor processing method of claim 21, further comprising

implanting an impurity into active areas of the transistors of the two series at the same moment

in time(Col.5, lines: 1-10).

67. Liou teaches the semiconductor processing method of claim 21, further comprising

implanting an impurity into active areas of the transistors of the two series at the same moment

in time to simultaneously define the different threshold voltages of the transistors of the two

series(Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that the substrate doping

effects the threshold voltage (Col.2, lines: 35-45)).

68 . Liou teaches the semiconductor processing method of claim 67, wherein the implanting of

the impurity is the only implant which defines the different threshold voltages of the transistors

of the two series ((Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that the

substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 69, Liou et al teaches wherein the common channel implant comprises

implanting a single type of impurity (P-Col.5, lines: 1-10)

In reference to claim 70, Liou et al teaches wherein the common channel implant comprises

implanting a single type of impurity to define the different Tvs of the transistors of the two series

(Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that the substrate doping effects

the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 71, Liou et al teaches wherein the transistors of the two series comprise

transistors having a single geometry type (Fig.2f)

In reference to claim 72, Liou et al teaches wherein the transistors of the single geometry type

comprise planar transistors (Fig.2f).

73. Liou teaches the semiconductor processing method of claim 26, further comprising

performing a common channel implant within active areas of the transistors of the two series at

the same moment in time (Col.5, lines: 1-10)

74. Liou teaches the semiconductor processing method of claim 26, further comprising

performing a common channel implant within active areas of both of the series of the transistors

at the same moment in time to define the different threshold voltages of the transistors of the two

series ((Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that the substrate doping

effects the threshold voltage (Col.2, lines: 35-45)).

75. Liou teaches the semiconductor processing method of claim 74, wherein the common

channel implant is the only channel implant which defines the different threshold voltages of the

transistors of the two series ((Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that

the substrate doping effects the threshold voltage (Col.2, lines: 35-45)).

76 . Liou teaches the semiconductor processing method of claim 26, further comprising

implanting an impurity into active areas of the transistors of the two series at the same moment

in time (Col.5, lines: 1-10)

77. Liou teaches the semiconductor processing method of claim 26, further comprising

implanting an impurity into active areas of the transistors of the two series at the same moment

in time to simultaneously define the different threshold voltages of the transistors of the two

series((Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that the substrate doping

effects the threshold voltage (Col.2, lines: 35-45)).

78. Liou teaches the semiconductor processing method of claim 77, wherein the implanting of

the impurity is the only implant which defines the different threshold voltages of the transistors

of the two series(Col.5, lines: 1-10).

In reference to claim 79, Liou et al teaches wherein the common channel implant comprises

implanting a single type of impurity (P-Col.5, lines: 1-10)

In reference to claim 80, Liou et al teaches wherein the common channel implant comprises

implanting a single type of impurity to define the different Tvs of the transistors of the two series

((Col.5, lines: 1-10- inherent-see Schuegraf et al ('976)- teaching that the substrate doping

effects the threshold voltage (Col.2, lines: 35-45)).

In reference to claim 81, Liou et al teaches wherein the active area widths individually

correspond to a dimension of an active area of respective FET between plural STI regions (STI)

immediately adjacent to opposing sides of the active are of the respective FET (Fig.2f)

In reference to claim 82, Liou et al teaches wherein the active area widths individually

correspond to a dimension of an active area of respective FET between plural STI regions (STI)

immediately adjacent to opposing sides of the active are of the respective FET (Fig.2f)
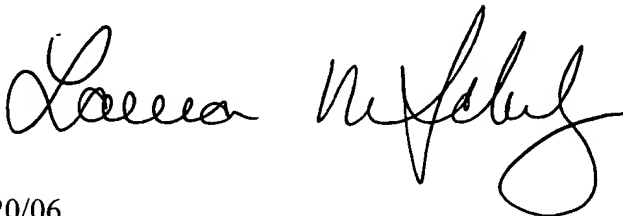
Conclusion

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697.

The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

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applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Laura M Schillinger
Primary Examiner
Art Unit 2813

07/20/06